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Claims 1-9 (cancelled)

10. A method of manufacturing a semiconductor device, the method comprising:

forming a gate electrode, having side surfaces, over an upper surface of a substrate with a gate dielectric layer therebetween;

forming a composite liner comprising:

an oxide liner on the side surfaces of the gate electrode and the upper surface of the substrate; and

a nitride liner on the oxide liner; and

forming a sidewall spacer on the composite liner.

11. The method according to claim 10, wherein:

the oxide liner comprises a silicon oxide;

the nitride liner comprises a silicon nitride; and

the sidewall spacer comprises a silicon oxide, silicon nitride or silicon oxynitride.

12. The method according to claim 11, comprising forming the sidewall spacer of a silicon oxide having a dielectric constant (k) no greater than about 3.9.

Claims 13-15 (cancelled)

16. The method according to claim 11, comprising ion implanting to form shallow source/drain extensions in the upper surface of the substrate, using the gate electrode as a mask, before forming the composite liner.

17. The method according to claim 16, comprising ion implanting a P-type impurity to form the source/drain extension.

18. The method according to claim 17, wherein the P-type impurity comprises boron.

19. The method according to claim 18, comprising forming the source/drain extensions at a junction depth (X_j) of about 200 Å to about 300 Å.